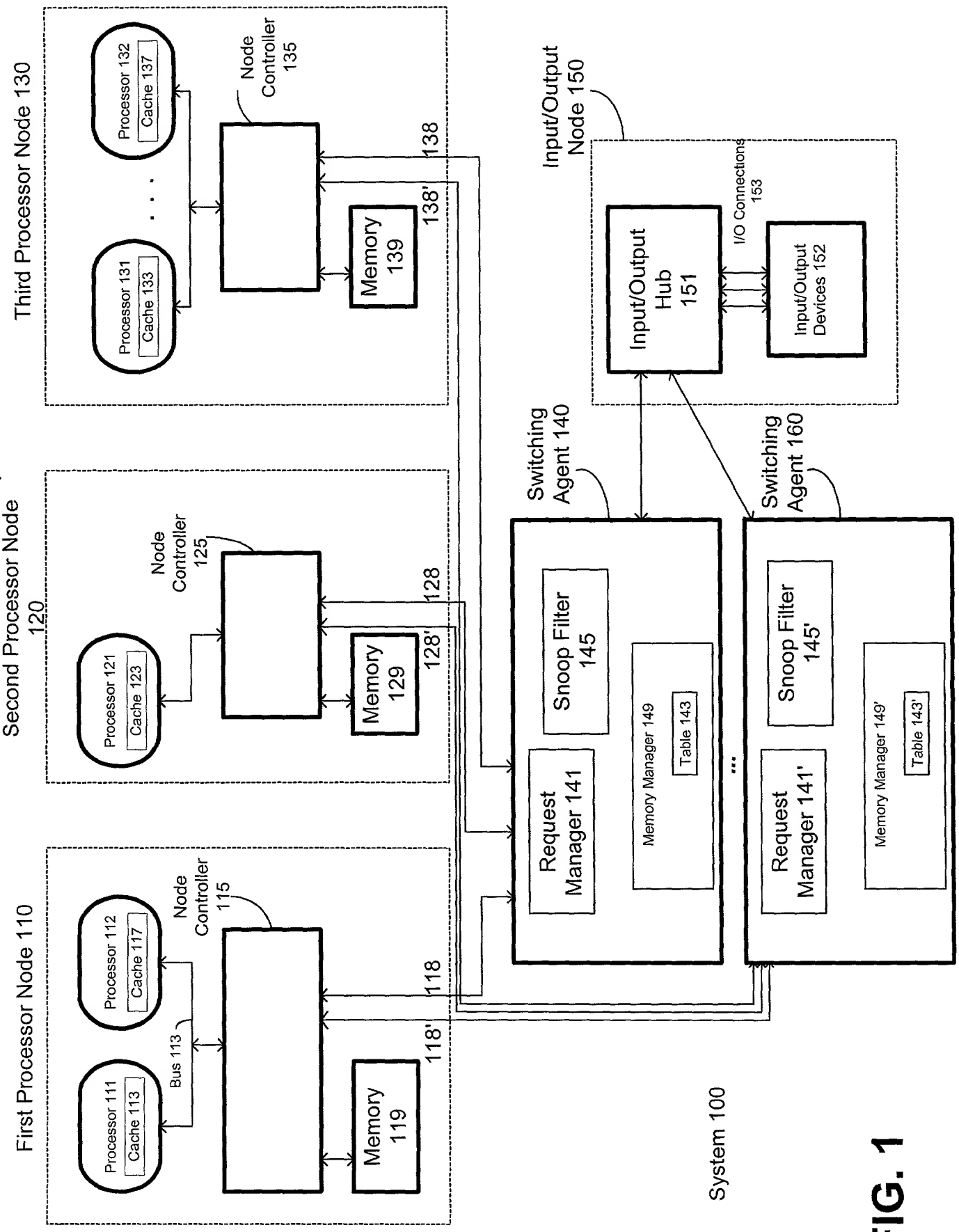

First Processor Node 110
Processor 111
Cache 113
Processor 112
Cache 117
Bus 113
Node Controller 115
Memory 119
118
118'
Second Processor Node 120
Processor 121
Cache 123
Node Controller 125
Memory 129
128
128'
Third Processor Node 130
Processor 131
Cache 133
Processor 132
Cache 137
Node Controller 135
Memory 139
138
138'
Switching Agent 140
Request Manager 141
Snoop Filter 145
Memory Manager 149
Table 143
Switching Agent 160
Request Manager 141'
Snoop Filter 145'
Memory Manager 149'
Table 143'
Input/Output Node 150
Input/Output Hub 151
I/O Connections 153
Input/Output Devices 152
System 100

FIG. 1

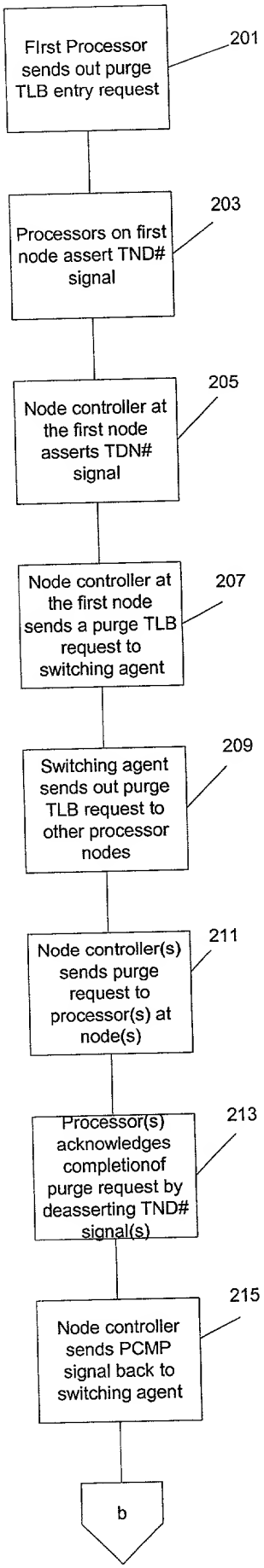
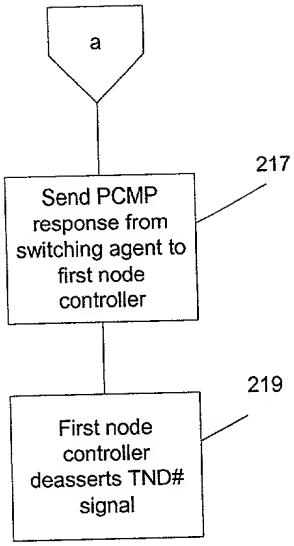

First Processor sends out purge TLB entry request
201
Processors on first node assert TND# signal
203
Node controller at the first node asserts TDN# signal
205
Node controller at the first node sends a purge TLB request to switching agent
207
Switching agent sends out purge TLB request to other processor nodes
209
Node controller(s) sends purge request to processor(s) at node(s)
211
Processor(s) acknowledges completionof purge request by deasserting TND# signal(s)
213
Node controller sends PCMP signal back to switching agent
215
b

Fig 2a


a
217
Send PCMP response from switching agent to first node controller
219
First node controller deasserts TND# signal